Alenkruth Krishnan Murali

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EDUCATION

Ph.D. in Computer Engineering GPA - 4.0/4.0 | *August 2022 - Present*
University of Virginia, Charlottesville, USA.

- Advisor: Dr. Ashish Venkat
- Coursework: Computer Architecture, Advanced Digital Logic Design, AI Hardware, and Hardware Security.
- Passed qualifying examination - Spring 2023.

Bachelor of Engineering - Electrical and Electronics Engineering GPA - 9.02/10.0 | *June 2017 - May 2021*
Anna University - PSG Institute of Technology and Applied Research, Coimbatore, India.

- Capstone Project: Optimized execution unit for RISC-V Packed SIMD Extension

RESEARCH INTERESTS

Computer Architecture - Micro-Architecture, Hardware Security, Hardware Accelerators and RTL Design.

EXPERIENCE

Graduate Research Assistant - Department of Computer Science, University of Virginia *August 2022 - Present*

- Building a reconfigurable RISC-V processor to deploy and test novel security verification techniques.

Graduate Teaching Assistant - Department of Computer Science, University of Virginia *August 2023 - Present*

- Graduate Computer Architecture with Dr. Adwait Jog. Responsibilities include creating and grading assignments and organizing office hours.

CPU Verification Engineer - Incore Semiconductors, India *June 2021 - May 2022*

- Functional verification of the RISC-V core generators designed at Incore Semiconductors.
- Developed a test generation framework for automatically generating assembly test programs to verify the microarchitecture.
- Developed an open verification framework using community-driven tools like cocotb and verilator.

RTL Design Intern - Incore Semiconductors, India *January 2021 - May 2021*

- Designed an optimized execution unit for the RISC-V Packed SIMD extension.
- Integrated the unit into the pipeline of a 2-stage RISC-V processor and tested it with assembly programs.
- The unit was integrated into the other core-generators designed in-house.

Research Intern - Indian Institute of Technology, Palakkad, India *May 2020 - August 2020*

- Worked under the guidance of Dr. Satyajit Das on “Extending RISC-V ISA to support Crypto Instructions”.
- Designed and integrated a low-area, low-power AES-256 accelerator into the pipeline of cv32e40p core.
- Created custom instructions and modified the RISC-V core to test the AES unit and the new instructions.

TECHNICAL SKILLS

PROGRAMMING LANGUAGES:	Python, C++, C.
HARDWARE DESCRIPTION LANGUAGES:	Verilog, Chisel, Bluespec System Verilog, SystemVerilog.
TOOLS:	Xilinx Vivado, Openlane, Questa, ModelSim, Git, Multisim.

PROJECTS

Core Fuzzing - A Versatile Platform for Security Verification *August 2022 - Present*

- Building a reconfigurable superscalar, out-of-order RISC-V core based on the BOOM core with Chisel to deploy and test security verification ideas.
- Implementing Dynamic Information Flow Tracking in the reconfigurable core.
- More details about this project can be found on my website.

RISC-V Packed SIMD Execution Unit *(Capstone Project at Incore Semiconductors)* *January 2021 - May 2021*

- Designed an execution unit to support the 32 and 64bit instructions in the Packed SIMD extension of RISC-V.

- Optimized the design across multiple iterations to reuse instantiated adders, shifters, and multipliers. The optimizations reduced the LUT slice utilization by 76%.
- Integrated the execution unit into the pipeline of a two-stage RISC-V microcontroller grade core and tested it with assembly programs.

Integrating an AES Accelerator with MicroBlaze Softcore Processor *February 2020 - May 2020*

- Modified and integrated an AES unit as a co-processor to Xilinx's MicroBlaze Soft Processor.
- The AES accelerator was interfaced with the CPU core through an AXI-Lite bus.
- The system was implemented on an Artix 7 FPGA development board, and the processor was programmed and tested with C programs.

MOM - A portable and Automatic Dosa, Idli, and Chapati maker *February 2020 - May 2020*

- Designed an efficient and reliable power supply, and motor control circuitry for the dosa making subsystem.
- The power supply was simulated on multisim. The motor control circuitry was implemented using Arduino Mega development boards and servo motors.

Implementation of a Basic Pipelined MIPS 32 processor *August 2019 - December 2019*

- Implemented a 5 stage MIPS 32 processor capable of executing 'R' type and 'I' type instructions as a study project.
- The verilog design was simulated using modelsim.

Domestic Energy Monitoring and Home Automation *August 2019 - December 2019*

- Designed a system that keeps track of the household energy consumption, graphs the data, estimates the bill amount, and displays the instantaneous data through an android application with minimal burden on the circuit.
- The system also provides a feature to automate the house through the same android application.

Tamil Text Classifier using PyTorch *May 2019 - July 2019*

- Developed a consonant - vowel classifier using a simple Convolutional Neural Network. The model can be improved to detect Tamil words on signboards.
- The project was done as a part of the PadhAI - Deep Learning course.

Gesture controlled Maze solver *January 2019 - March 2019*

- Designed an ATmega328P based maze solver controlled by an android application.
- The application transmits the phone's accelerometer and gyroscope readings which the controller interprets to actuate a pair of servo motors.

TALKS AND PRESENTATIONS

TECHCON (2023) - SRC

- Invited to present our work Core Fuzzing in Semiconductor Research Corporation's annual conference.

USING UATG AND RIVER CORE TO FIND BUGS IN CHROMITE (2021) - INCORE SEMICONDUCTORS

- As the industry liaison and TA for the course, I introduced senior undergraduate students to the microarchitecture of Chromite, the microarchitectural test generation framework (UATG), and the co-simulation framework (RIVER CORE) and helped them find functional bugs in the design with the tools.

EMBEDDED SYSTEMS USING TI MSP432 WORKSHOP (2020) - PSGiTECH

- Designed, coordinated, and instructed a two-day workshop on using MSP432 boards for embedded system development in an inter-college symposium.

HONORS AND AWARDS

- **Academic Excellence** - Ranked 15 out of 9542 students in the state *2021*
- **Best Outgoing Student** - Awarded to one student from each department for excellence *2021*
- **Rajya Puraskar** - The Bharat Scouts & Guides *2016*

ACTIVITIES

- **Steering Committee Member and Social Chair** - Computer Architecture Student Association *Nov 2022 - Present*
- **Chairman** - EEE Association, PSG iTech *September 2020 - August 2021*

OTHER COURSES AND CERTIFICATIONS

- uArch Workshop - ISCA 2022, ISCA 2021 [virtual participation] (Invited Student) *(2022)*
- Xilinx HPC Workshop - ISCA 2021 (*2021*)
- Introduction to Linux - LFS101x (*2021*)
- ACACES Virtual Summer School - HiPEAC (*2020*)
- Data Structures (C++, Python) (*2020*)
- HDL for FPGA Design (*2020*)
- Hardware Modeling using Verilog (*2019*)
- Computer Architecture Winter School - PES University, India (*2020*

References available upon request